## CLAIMS

1. A receiver/decoder comprising:

at least one port for receiving messages;

a memory including a FIFO section;

at least one application module; and

FIFO control means coupled to the or each port, the memory, and the or each application module operative in response to a message appearing at a port to write the message into the FIFO section of the memory and to read the message from the FIFO section of the memory out to an application module or to a further port.

2. A receiver/decoder according to claim 1 wherein the FIFO control means is arranged to initiate the reading out of a message from the FIFO section of the memory to said application module or to said further port before receipt of the message is complete.

3. A receiver/decoder according to claim 1 ~~or 2~~ wherein the FIFO control means includes occupancy detector means for detecting the state of occupancy of the FIFO.

4. A receiver/decoder according to claim 3 wherein the occupancy detector means is adapted to detect overflow and underflow of the FIFO.

5. A receiver/decoder according to either of claims 3 ~~and 4~~ wherein the occupancy detector means is adapted to detect at least one threshold of impending overflow and underflow of the FIFO.

6. A receiver/decoder according to ~~any preceding~~ claim 1 wherein the FIFO control means is arranged to flush a message from the FIFO section.

7. A receiver/decoder according to ~~any preceding~~ claim 1 wherein the FIFO section comprises a plurality of FIFO buffers and the FIFO control means comprises a respective plurality of FIFO register control means.

8. A receiver/decoder according to ~~any preceding~~ claim 1 wherein the memory further includes a buffer section, and the receiver/decoder includes buffer control means operative in response to a message appearing at a port to write the message into the buffer section of the memory and in response to a control signal from an application module to read the message from the buffer to the application module.

9. A receiver/decoder according to Claim 8, wherein the buffer section comprises two buffers areas defined by respective buffer registers in the buffer control means.

10. A receiver/decoder according to Claim 9 wherein the buffer control means is operable in a bit stream mode in which an incoming bit stream is directed into the currently selected buffer area and is then switched between the two buffer areas as each buffer area in turn becomes full.

11. A receiver/decoder according to Claim 9 ~~or 10~~ wherein the buffer control means is operable in a datagram mode in which the length of an incoming message is compared with the free space in the currently selected buffer area, and if that space is less than the length of the message, the other buffer area is selected.

12. A receiver/decoder according to ~~any preceding~~ claim 1 including a video device application unit fed from the FIFO section and feeding a chip unit which is also fed with a video bitstream.

13. A broadcast system comprising a receiver/decoder according to ~~any preceding~~ claim 1 and means for transmitting messages to the receiver/decoder.

14. A receiver/decoder substantially as herein described.

15. A broadcast system substantially as herein described.